

Fig. 1

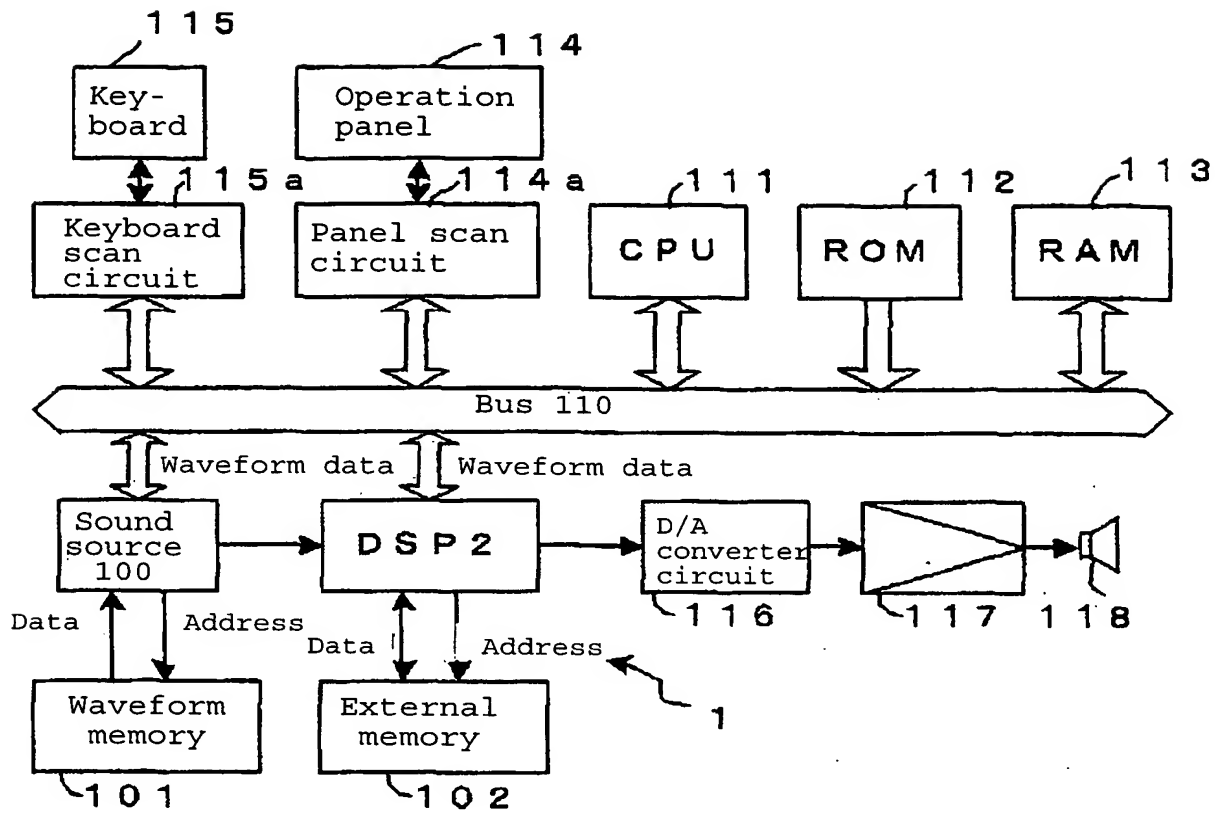
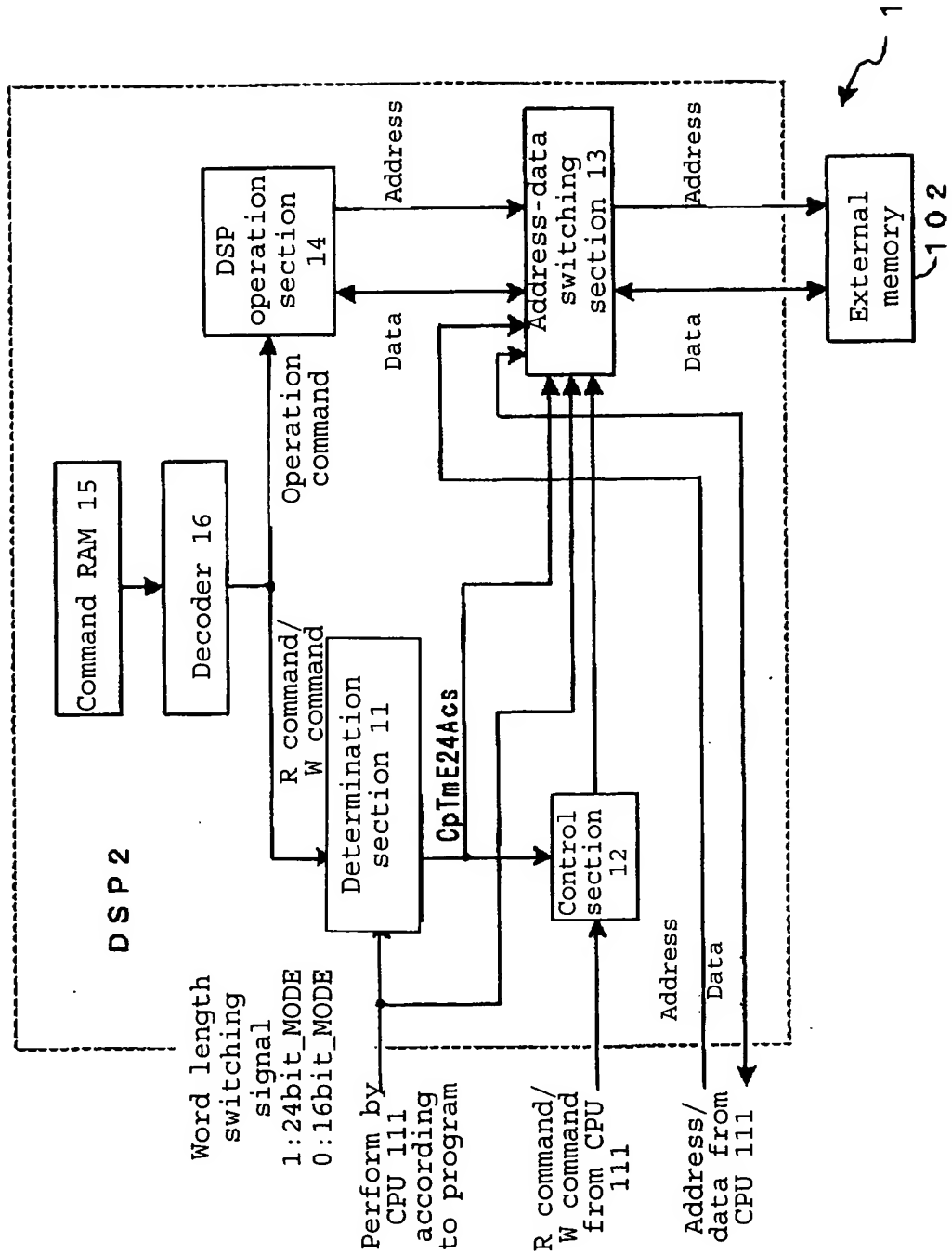
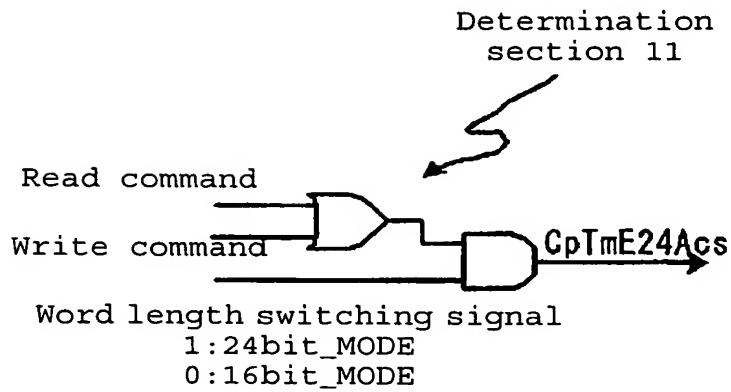


Fig.2



**F i g.3**



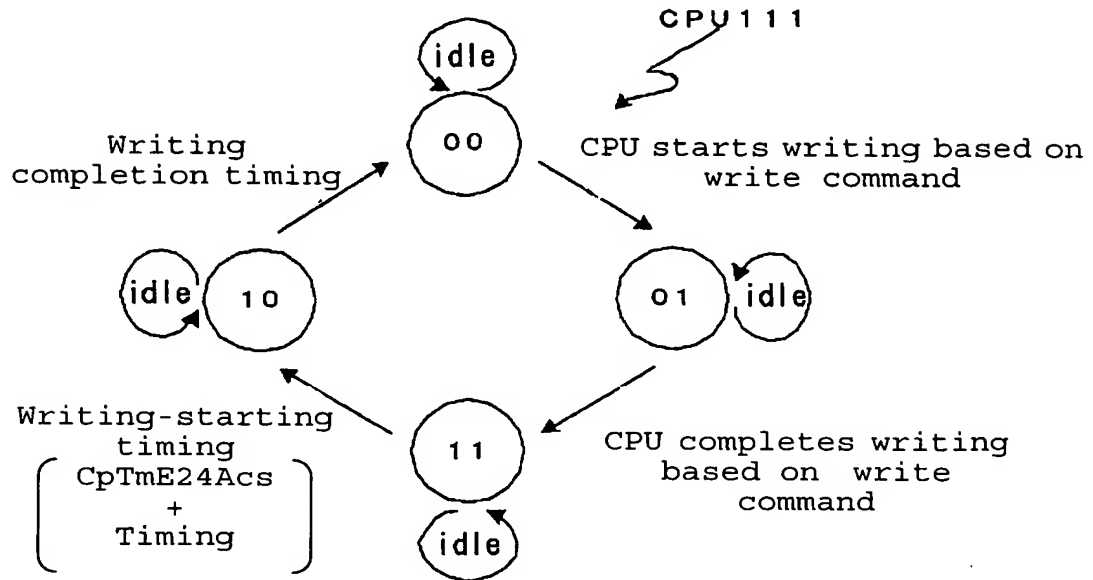
**F i g.4**

CpTmE24Acs		
24bit _MODE (1)	R	1
	W	1
	N	0
16bit _MODE (0)	R	0
	W	0
	N	0

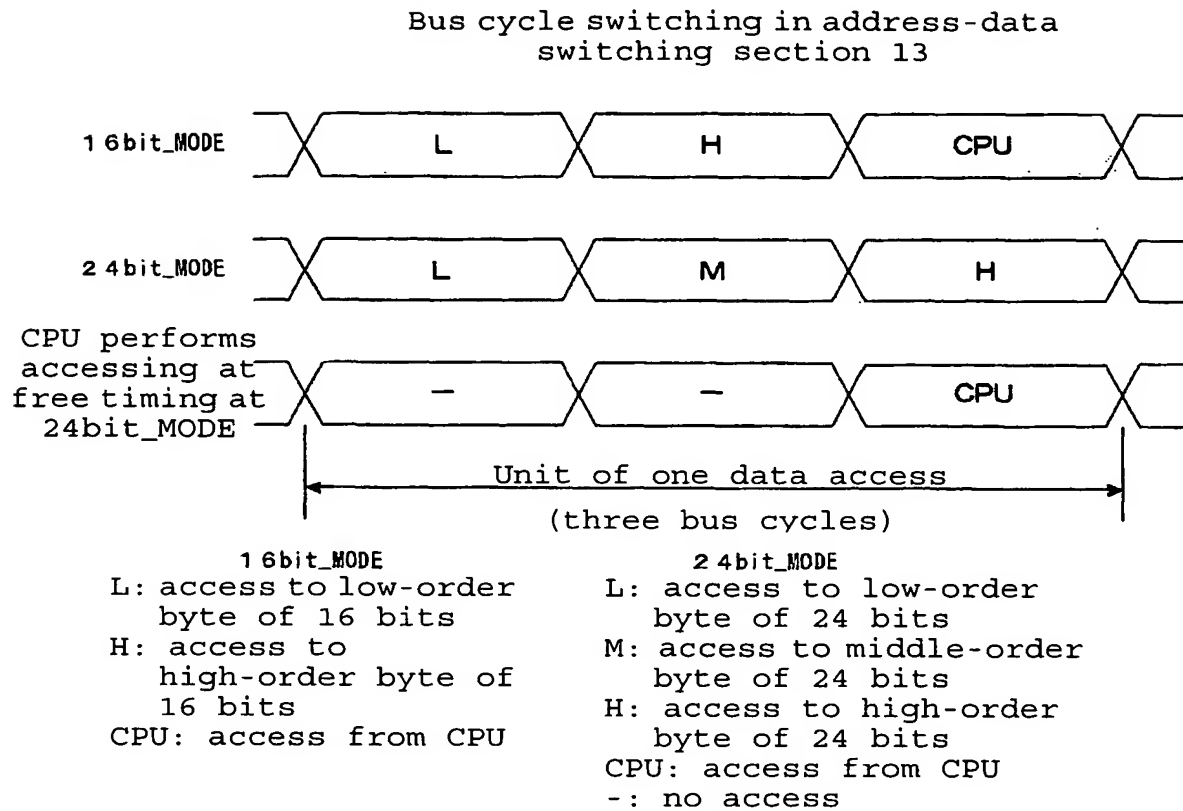
CpTmE24Acs = 0  
When CPU 111 is  
allowed to access

**F i g.5**

State machine for controlling access from  
CPU 111 to external memory 102  
(case of writing)



**F i g.6**



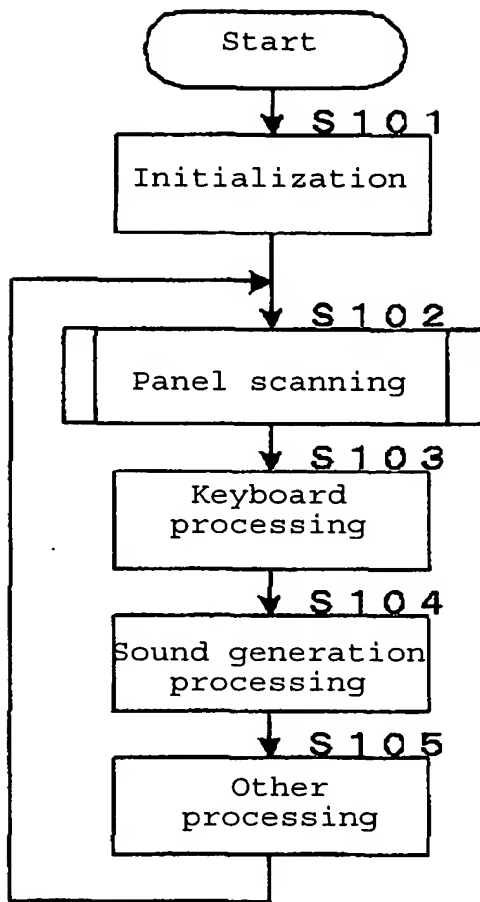
**Fig. 7**

Fig. 8

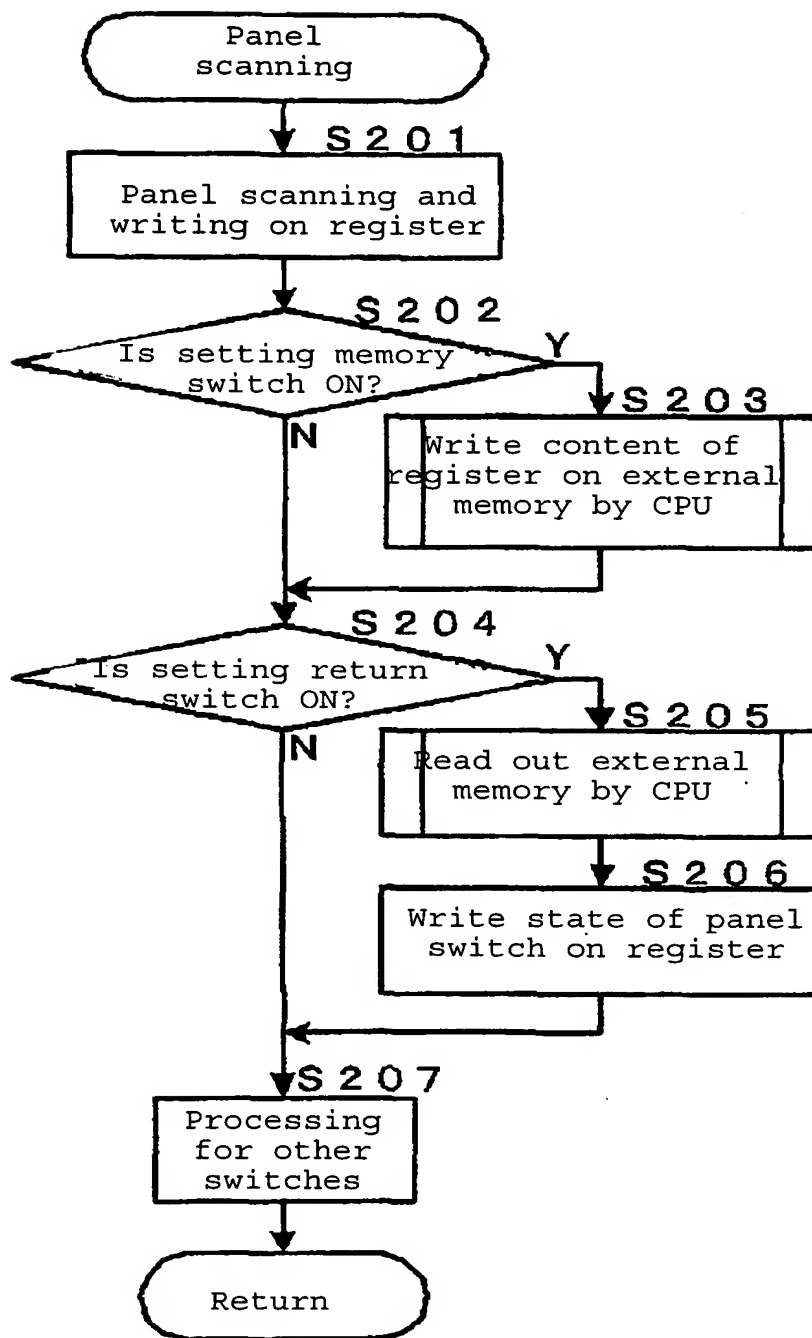


Fig. 9

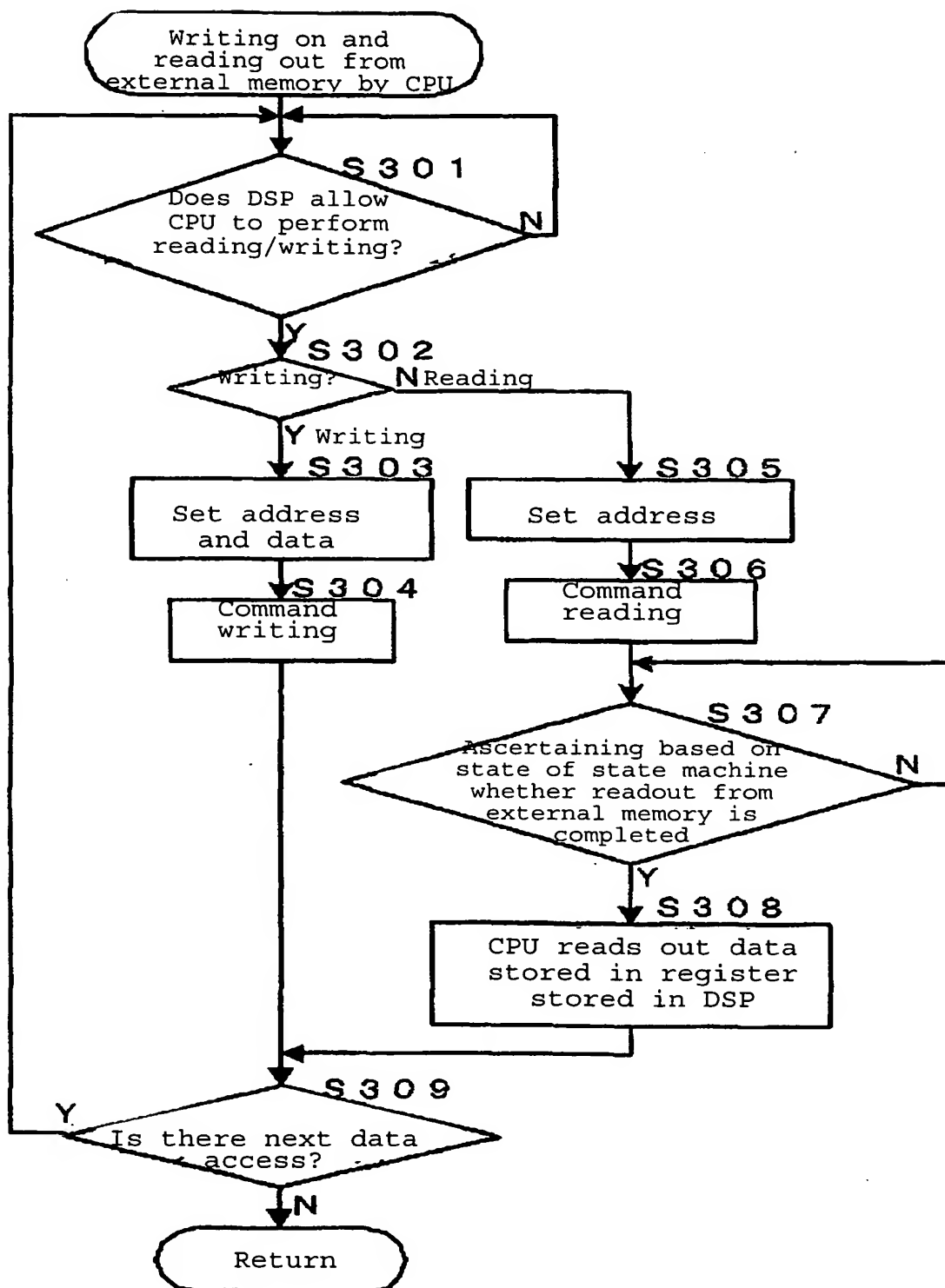


Fig. 10

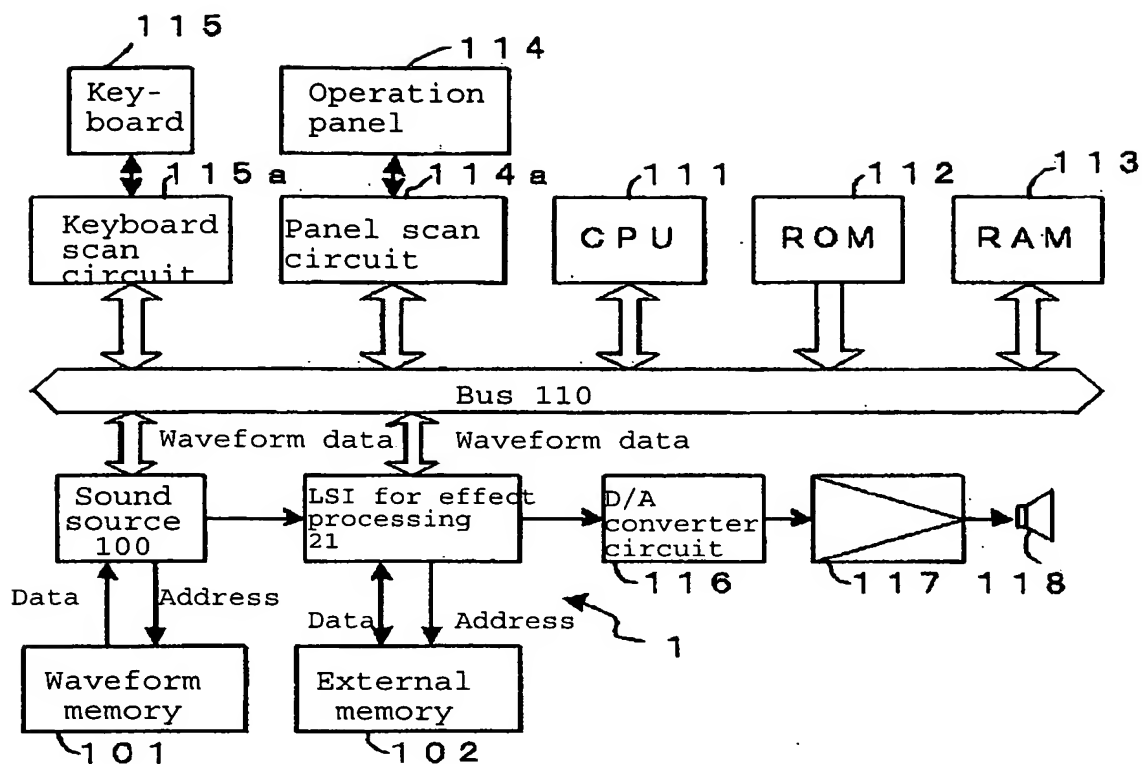


Fig. 11

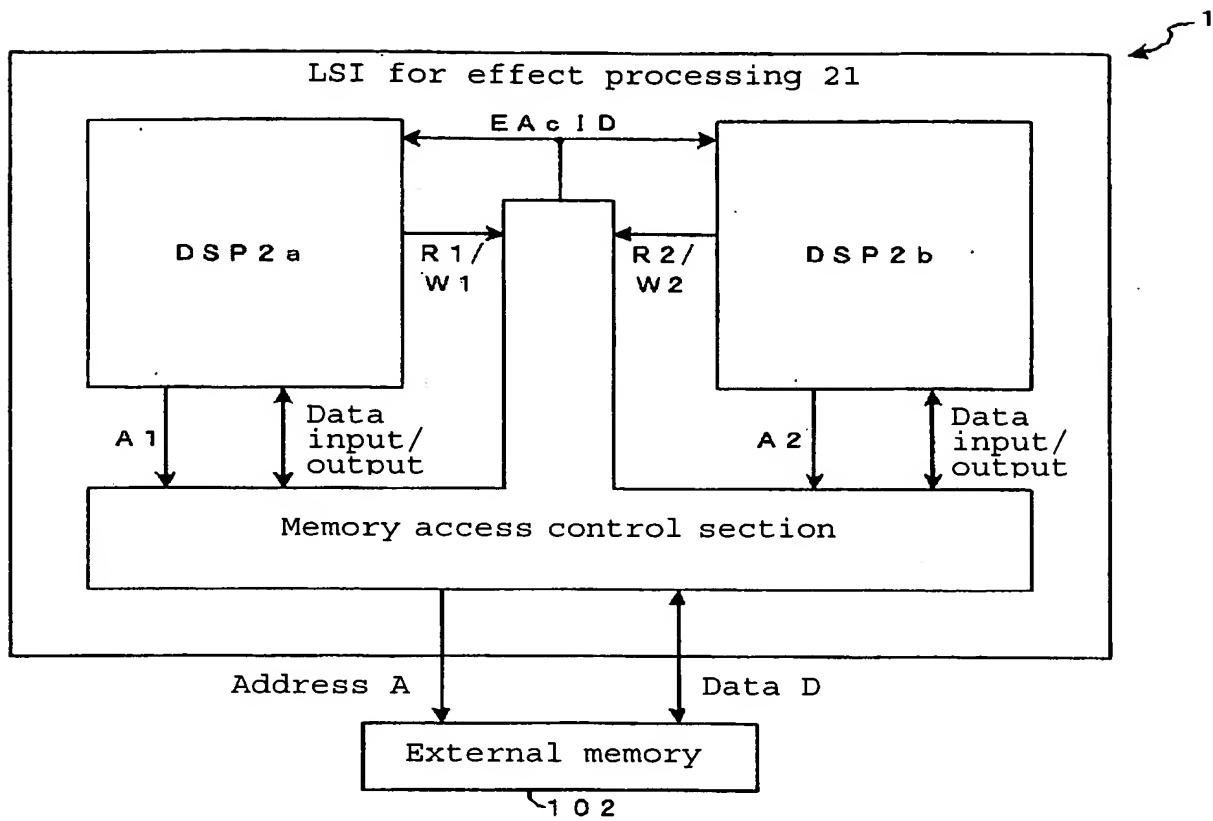
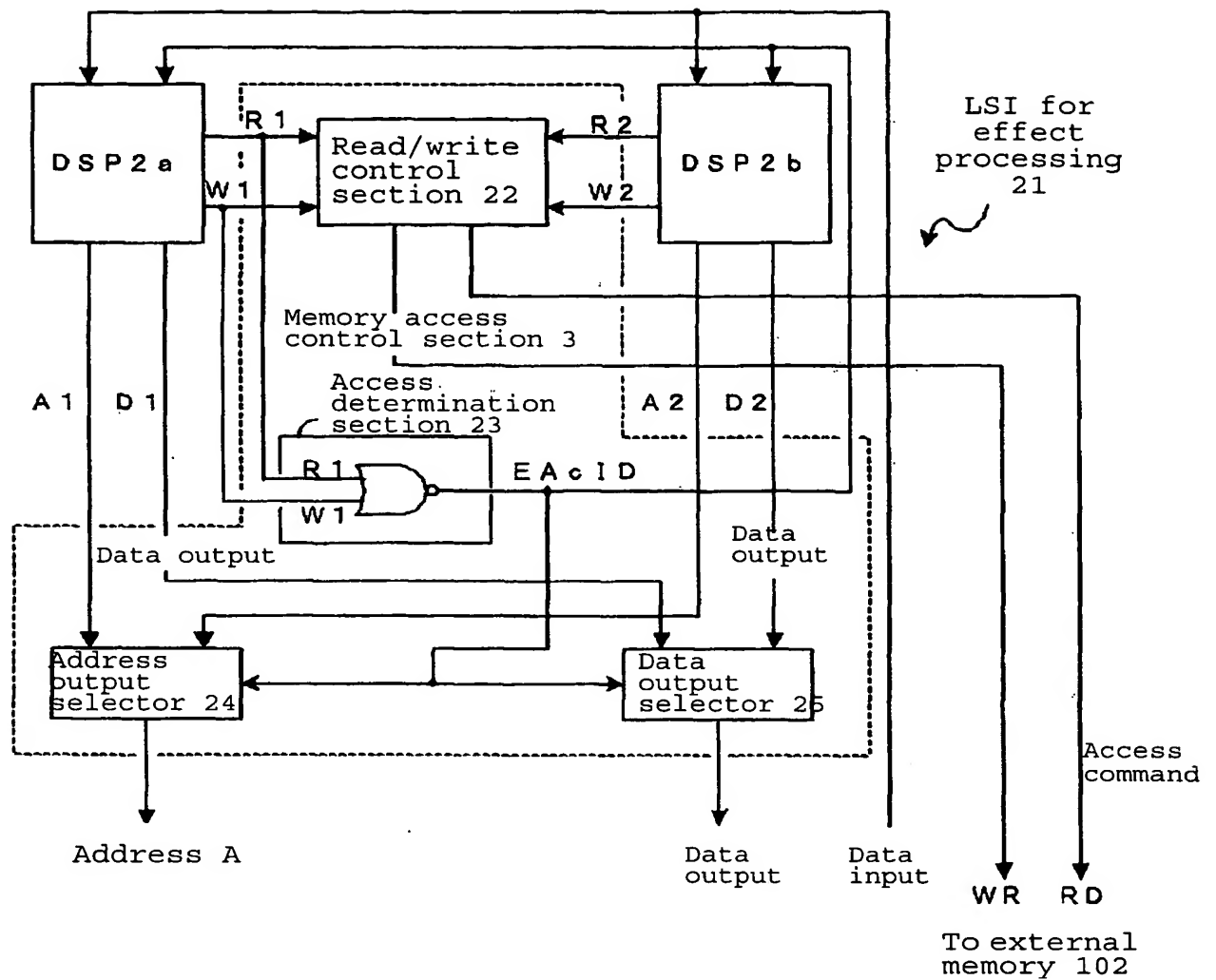


Fig. 12



**Fig.13**

DSP2 a	DSP2 b	After control
R1	R2	N
R1	W2	N
R1	N	R1
W1	R2	N
W1	W2	N
W1	N	W1
N	R2	R2
N	W2	W2
N	N	N

R: read  
W: write  
N: no access

**Fig.14**

R1	W1	EA c ID
0	0	1 DSP2 b
1	0	0 DSP2 a
0	1	0 DSP2 a

Fig. 15

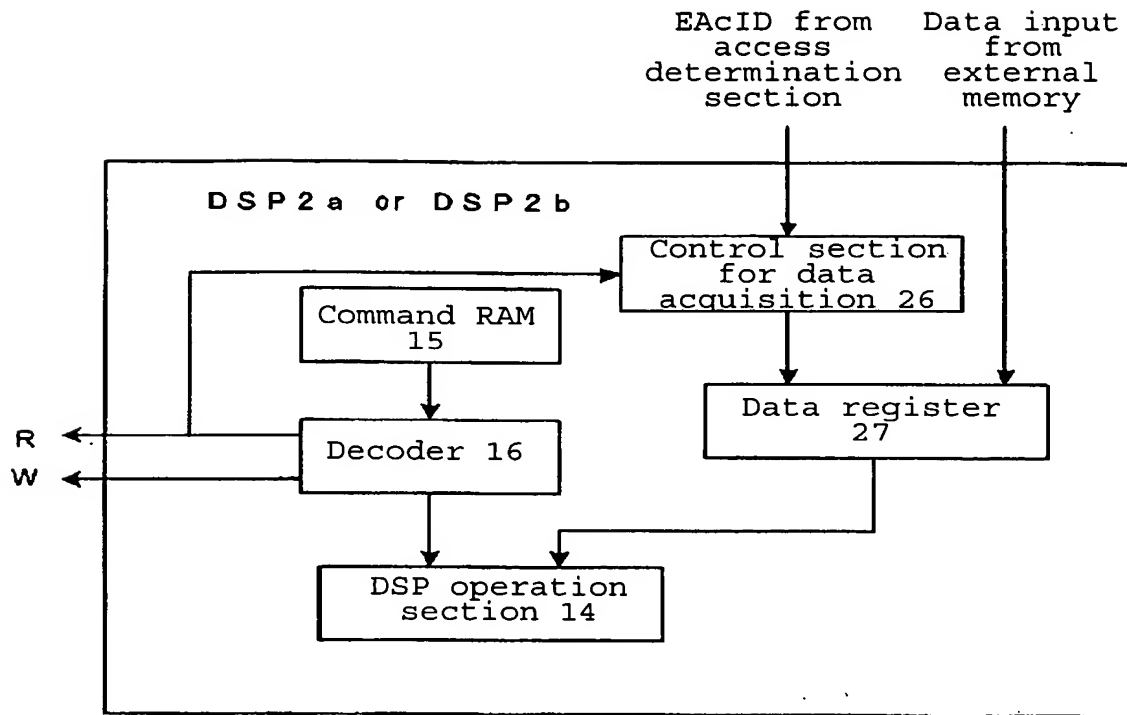


Fig. 16

	1	2	3	4	5	6	7	8	.....
DSP 2 a	R1	R1	N	N	W1	N	R1	N	.....
DSP 2 b	N	N	R2	W2	N	N	N	N	.....
After control	R1	R1	R2	W2	W1	N	R1	N	.....

Fig. 17

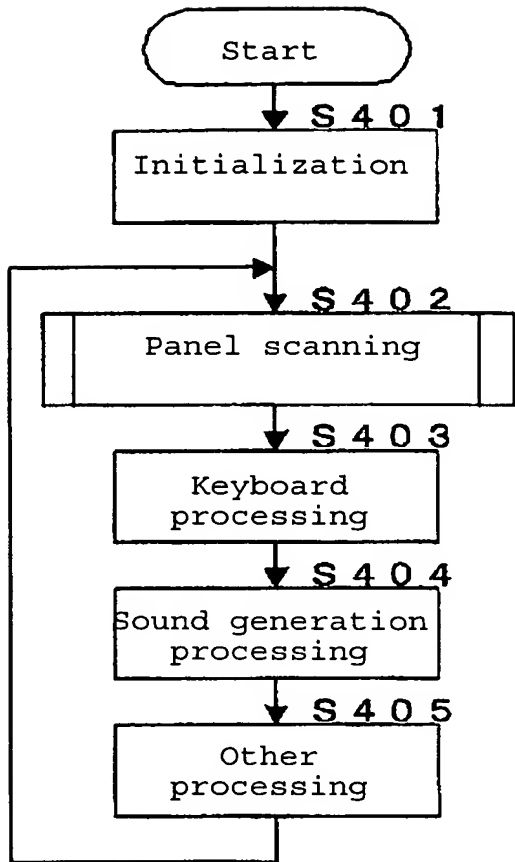


Fig. 18

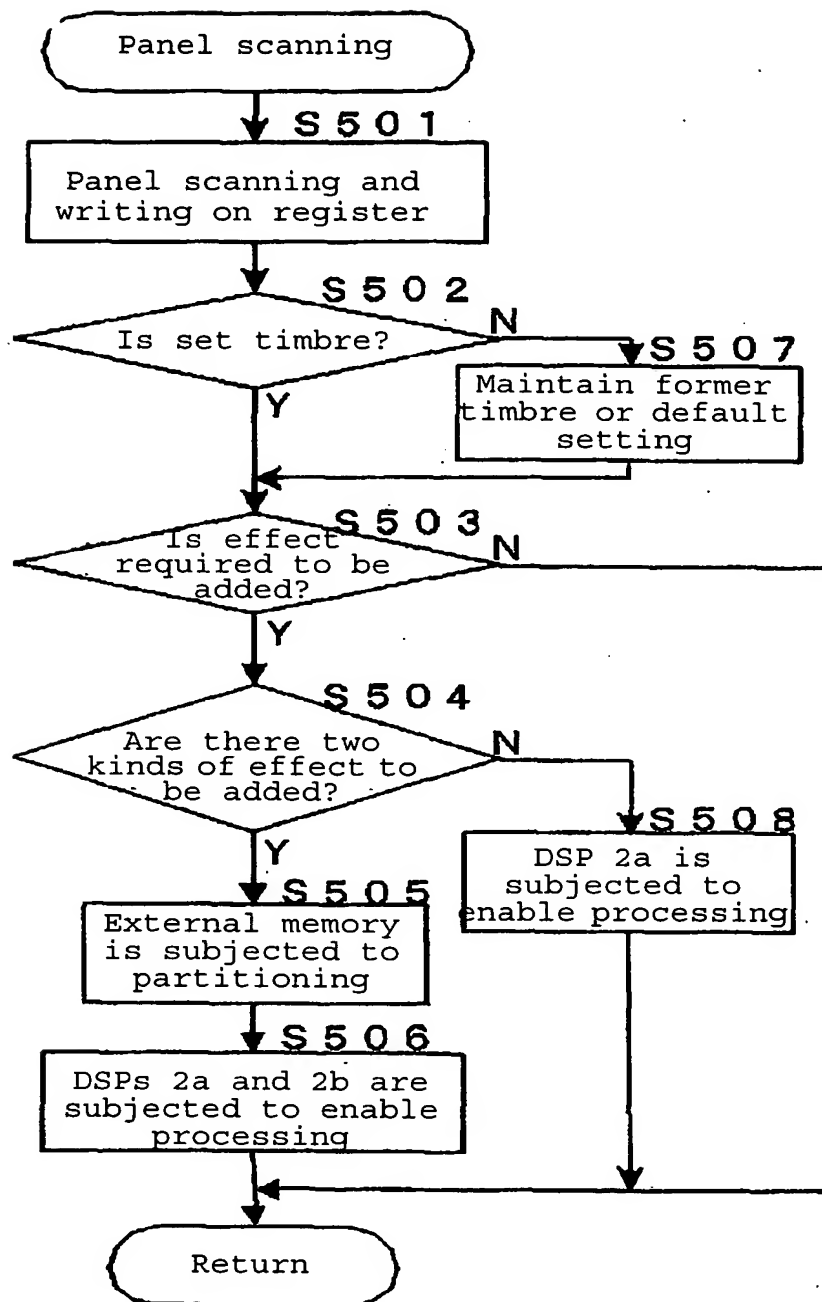
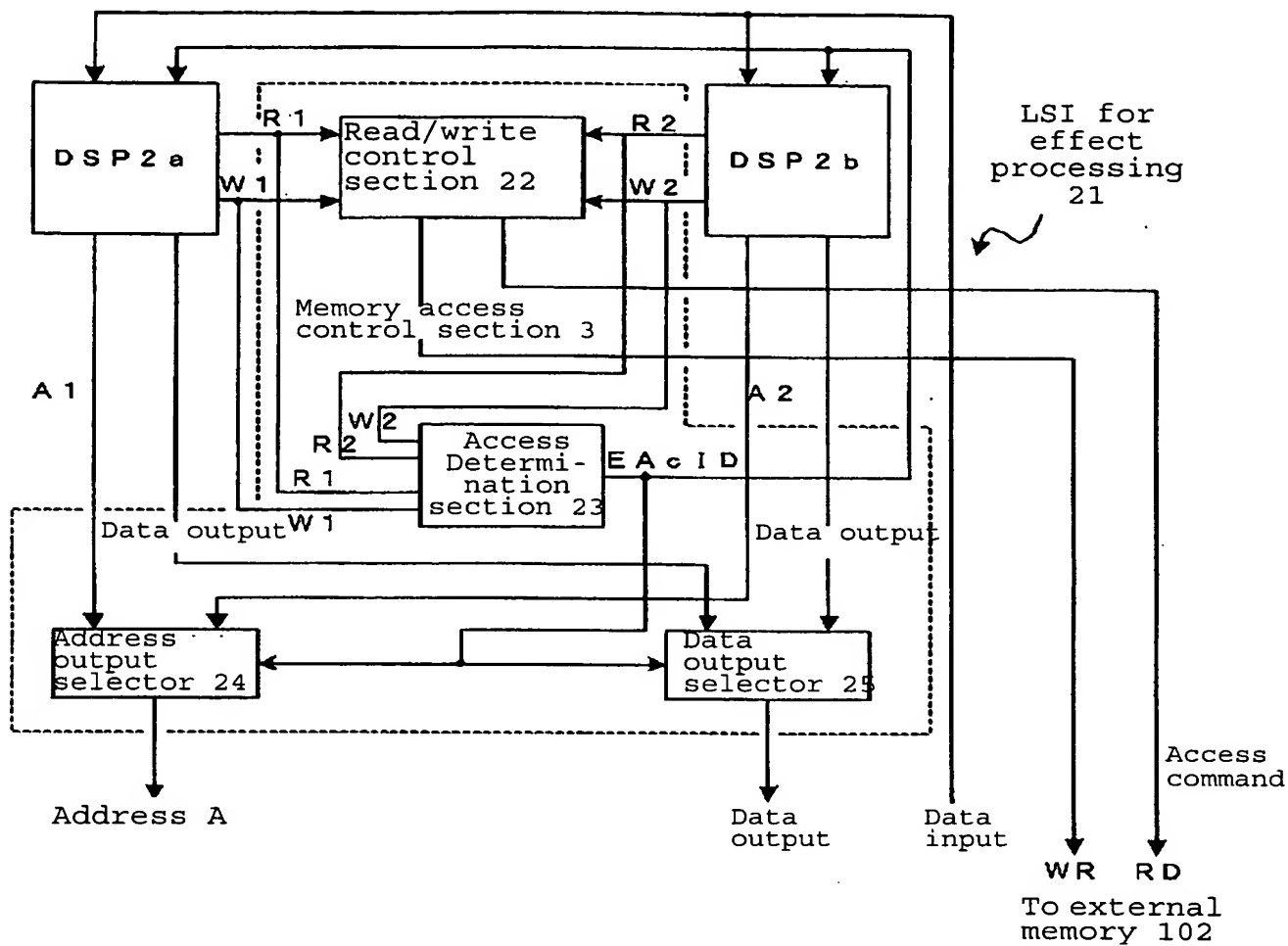


Fig. 19



Timing when access to external memory 102 is available

1 2 3 63 64

One sampling cycle (44.1 KHz)